Amendments to the Specification:

Please replace paragraph [0004] of the specification with the following amended paragraph:

Please refer to Fig.1, which is a block diagram of a prior art computer system 10. The computer system 10 includes a central processing unit (CPU) 12, a north bridge circuit 14, a system memory 16, a display controller 18, and a monitor 20. The CPU 12 is used to control operation of the computer system 10. The north bridge circuit 14 is used to arbitrate signal transmission among the system memory 16, the display controller 18, and the CPU 12. The system memory 16 is used to store computational data of the CPU 12, and the display controller 18 is used to output video signals for driving the monitor 20 to show corresponding images. The display ~~control~~ controller 18 includes a graphics chip 22, a video memory 24, and a digital-to-analog converter (DAC) 26. In addition, the video memory 24 has a computation buffer (a Z-buffer or a texture buffer for example) 28 and a frame buffer 30. The graphics chip 22 is capable of processing 2D and 3D graphics data, and stores the calculation results in the computation buffer 28. In addition, the graphics chip 22 stores display data (gray levels for instance) corresponding to the pixels of the monitor 20 in the frame buffer 30. Then, the DAC 26 converts the display data (digital signals) into corresponding display driving voltages (analog signals), and outputs the display driving voltages to the monitor 20 for driving the pixels to show corresponding images.

Please replace paragraph [0032] of the specification with the following amended paragraph:

Generally speaking, the state machine 78 is built by a plurality of flip-flops. As shown in Fig.5, after ~~After~~ the state machine [[96]] 78 enters the operational state 96, the state machine stays in the operational state 96 for ~~, therefore, stops flip-flops from being triggered to achieve the objective of~~ holding the setting value SET. When the DAC 66 starts converting the digital display data into analog display driving voltages,

the setting value SET controls the mirror ratio 76 to adjust the display driving voltages corresponding to different gray levels. In the preferred embodiment, the mirror ratio setting units 88a, 88b, 88c of the mirror ratio controller 76 respectively correspond to different W/L ratios. Therefore, the mirror ratio setting units 88a, 88b, 88c have different adjustment magnitude for the reference current Iref'. However, the mirror ratio setting units 88a, 88b, 88c are capable of having the same W/L ratio for tuning the reference current Iref'. That is, the total number of the selected mirror ratio setting units dominates the reference current Iref'. Therefore, more mirror ratio setting units are increased to lower the reference current Iref' when the setting value SET is increased, and fewer mirror ratio setting units are decreased to boost the reference current Iref' when the setting value SET is decreased.